

Co-design of On-chip Antennas and Circuits for a UNII Band Monolithic Transceiver

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Introduction

The surge of highly integrated and multifunction wireless devices has necessitated the designers to think outside the box for solutions that are unconventional. The new trends have provided the impetus for low cost and compact RF System-on-Chip (SoC) approach [1]. The major advantages of SoC are miniaturization and cost reduction. A major bottleneck to the true realization of monolithic RF SoC transceivers is the implementation of on-chip antennas with the circuits. Though completely integrated transceivers with on-chip antennas have been demonstrated but generally these designs are for high frequencies. Moreover, they either use non-standard CMOS processes or additional fabrication steps to enhance the antenna efficiency, which in turn adds to the cost of the system [2-3]. Another challenge related to the on-chip antennas is the characterization of their radiation properties. Most of the recently reported work (summarized in Table I) shows that very few on-chip antenna designs are characterized for their radiation patterns. Our previous work [4], demonstrated a Phase Lock Loop (PLL) based transmitter (TX) with an on-chip antenna. However, the radiation from the on-chip antenna experienced strong interference due to 1) some active circuitry on one side of the chip and 2) the PCB used to mount the chip in the anechoic chamber. This paper presents a complete 5.2 GHz (UNII band) transceiver with separate TX and receiver (RX) antennas. To the author's best knowledge, its size of 3 mm² is the smallest reported for a UNII band transceiver with two on-chip antennas. Both antennas are characterized for their radiation properties through an on-wafer custom measurement setup. The strategy to co-design on-chip antennas with circuits, resultant trade-offs and measurement challenges have been discussed.

Design: Transceiver with on-chip antennas

The design employs the standard 0.13 μm CMOS process. The monolithic transceiver with on-chip antennas is shown in Fig. 1. The TX comprises a voltage-controlled oscillator (VCO), where the resonant tank inductor has been optimized to radiate as an antenna. Loop antenna topology has been chosen due to its inductive nature. In this design, VCO is placed inside the loop antenna and care has been taken that the antenna remains close to the chip edges with minimum interference from the active circuitry. The antenna has been modeled in Ansoft HFSS as shown in Fig. 2. The simulation setup includes two lumped ports feeding the bond pads, connecting lines and a metal block representing the VCO. The antenna/inductor sizes 1 x 0.5 mm and produces a radiation pattern similar to an electrically small loop antenna (maximum along the plane of the loop). Differential impedance is extracted from the two port S-parameters, which demonstrates an inductance of 1.4 nH and a Q of 14 at 5.2 GHz. The differential impedance from the antenna is then utilized in Cadence to design the VCO.

On the RX side, a dipole antenna is realized which is conjugate matched to the input impedance of the differential Low Noise Amplifier (LNA). In order to match the large real part of the LNA impedance ($91+j 124 \Omega$), the dipole's length is increased which results in a folded structure as shown in Fig. 1. This, however, mostly increased the loss resistance instead of the radiation resistance and resulted in reduced antenna gain. It is worth mentioning here that the co-design of antenna and LNA eased the matching process as the antenna and the LNA were tuned simultaneously in EM and circuit simulators, respectively, to achieve a balance between conjugate matching and their individual performances. Finally, a wide-band match is obtained between the two as shown by the impedance curves in Fig. 3. The circuits are placed inside the antenna and their details can be found in [5].

Table I: Comparison with latest on-chip antenna work

Ref	Freq GHz	Antenna Type	Co-design of circuits	Process	Chip Size	Radiation Pattern
6	22-29	Monopole	No	Non-standard high res Si	6 inch wafer	Simulated
7	6-10	Monopole	TX	Standard low res Si based CMOS	6 mm ²	Simulated
2	94	Log-periodic	No	Non-standard high res GaAs	3.1 mm ²	Measured
8	60	PIFA	No	Standard low res Si based CMOS	0.57 mm ²	Simulated
9	24/60	Monopole	No	Standard low res Si based CMOS	0.8 mm ²	Simulated
10	5	Slot	RX	Standard low res Si based CMOS	4 mm ²	Not given
This work	5	Loop and dipole	TX/RX (two antennas)	Standard low res Si based CMOS	3 mm ²	Measured

Layout Challenges

Due to highly integrated design, in particular the placement of circuits inside the antenna, the layout becomes quite challenging. Fitting many inductors in a small area without affecting the performance of circuits and the antenna is quite complicated. Care is taken that the inductors are laid down in a manner that their currents are in opposite direction so as to minimize the mutual coupling between them. Guard rings are made around every circuit block to avoid substrate coupling. Metal fill is another difficult task, which is done with the aid of EM simulations to avoid parasitic coupling effects on the antenna. Since on-chip antennas are not typically part of a CMOS process, many design rules are violated by its inclusion. An example of such error is the violation of an antenna rule where a large metal in the top layer cannot be connected directly to a transistor. To avoid this, one end of the antenna is connected to the ground but with the provision of a microsurgery point. This ground connection must be removed through lasers before any testing can be performed on the chip. Similar microsurgery points are included to facilitate independent testing of the sub-modules.

Measurements and Results

The on-chip antennas gain and radiation pattern are measured with the same technique as described in [4], however, this time the chip is not mounted on a PCB. Instead, the measurements are done on a bare die glued to a glass plate with a direct feed from the RF probe, as shown in Figure 4. A custom stand is used to measure the radiated power at

different angles and the scanning is done manually. A measured gain of -22 dB is achieved for the TX antenna. The measured radiation pattern is shown in Figure 5. The maximum radiation is achieved along the plane of the loop ($\pm 90^\circ$), as expected. This confirms the validity of the design precautions applied to this chip. There is, however, still a difference of 3 to 4 dBs between the levels of each radiation pattern peak. The asymmetry can be attributed to measurement error, namely the presence of metal obstructions at $+90^\circ$. Though the gain is low, it is sufficient to communicate for 2 m with a RX connected to an off-chip antenna, as has been demonstrated in [4]. For the RX antenna, same setup is used as the TX antenna but since the output is taken from the LNA, its gain has to be subtracted in order to isolate the antenna gain. A gain of -35 dB is measured with the bore-sight maximum radiation pattern as shown in Fig. 6. The measured result is consistent with the simulated radiation pattern of the dipole antenna.

Conclusion

A UNII band monolithic transceiver with two on-chip antennas has been demonstrated. The complete chip, sized 3 mm^2 , is the smallest reported for such a configuration. The antenna on the TX side performs double duty by providing the inductance to the VCO resonant tank. On the other hand, the RX side antenna has been conjugate matched to the LNA. Through a co-design strategy, the circuits have been placed inside the antennas to demonstrate an efficient use of the chip-space. Many layout challenges have been highlighted for such an integrated design. Both antennas have been characterized for their radiation properties through a custom on-wafer setup.

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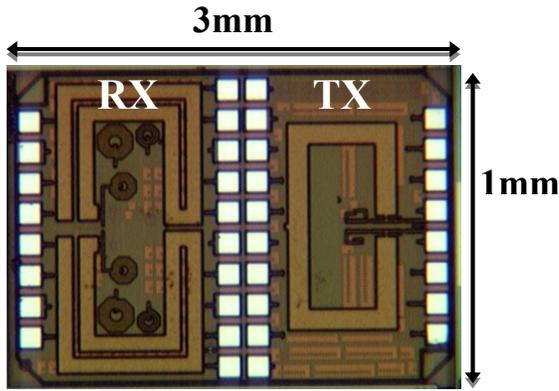


Fig. 1 Transceiver microphotograph

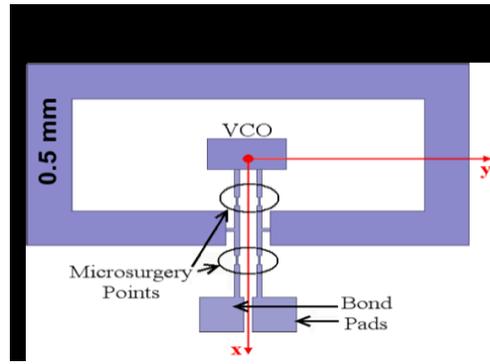


Fig. 2 TX on-chip antenna HFSS model

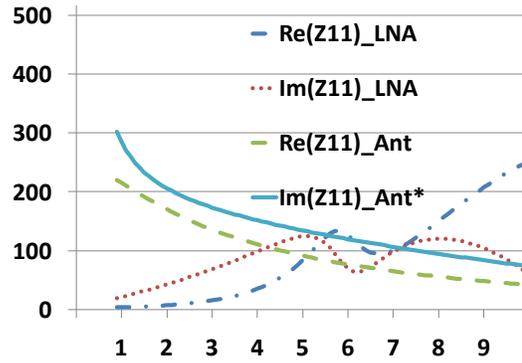


Fig. 3 RX on-chip antenna and LNA impedance

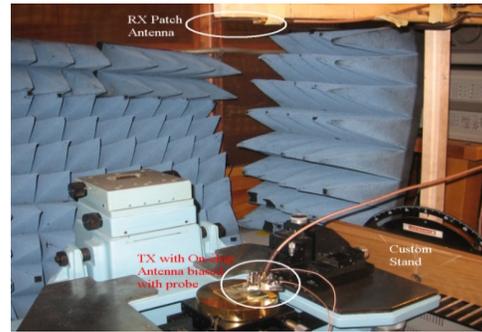


Fig. 4 On-chip antenna measurement setup

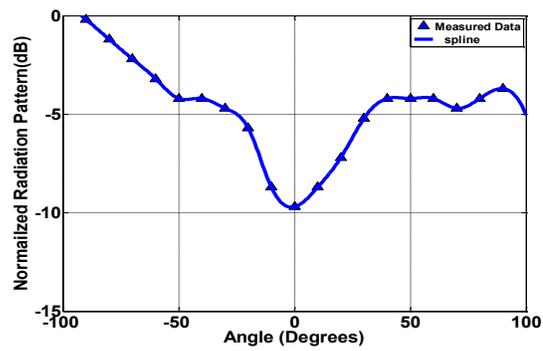


Fig. 5 TX on-chip antenna radiation pattern

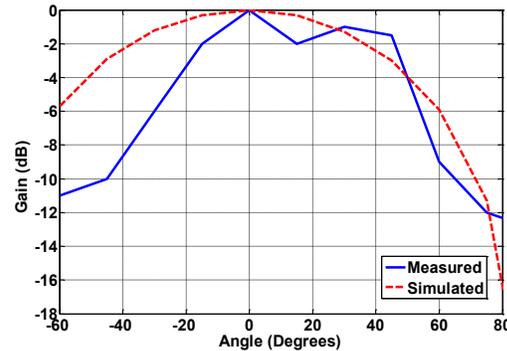


Fig. 6 RX on-chip antenna radiation pattern